Evaluation of Built-In Test

M. PECHT
M. DUBE
M. NATISHAN
University of Maryland
R. WILLIAMS
J. BANNER
I. KNOWLES
Defense Procurement Agency
England

Built-in test (BIT) provides fault finding as a means to aid in system assembly, test, and maintenance. An investigation to evaluate BIT of a particular electronics board used in the in-flight entertainment system for Boeing 777s is described. We found BIT proved useful when failure occurrences were uniquely associated with the operating environment, situations which can result in no-fault found, or could-not duplicate (CND) failures upon test. We also observed cases where the BIT failed to observe failures, and in some cases pointed to the wrong cause of failure. These and other advantages and disadvantages of BIT implementation are discussed.

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Authors' addresses: M. Pecht, M. Dube, M. Natishan, CALCE–Electronic Products and Systems Center, University of Maryland, College Park, MD 20742; R. Williams, J. Banner, I. Knowles, Defence Procurement Agency, Abbey Wood, Bristol BS34 8JH UK.

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INTRODUCTION

Over the last decade, the increasing complexity of electronic equipment, especially in low volume complex electronic systems, such as military, aerospace, and automotive applications, has resulted in an increased need to provide in-situ fault finding capabilities [1]. Built-in test (BIT) is defined as an on-board hardware-software diagnostic means to identify and locate faults and includes error detection and correction circuits, totally self-checking circuits, and self-verification circuits [24].

The usefulness of BIT in electronic equipment was recognized as early as the 1950s [2]. The objective was to ensure uninterrupted availability and fault free operation of critical weapons systems (Minutemen I and II missiles) and aerospace equipment (Saturn, Apollo). While BIT has historically been used for in-field maintenance by the end user, it has also been used to indicate system status [3], and to indicate whether a system has been assembled properly. As a result, BIT has been used in diverse applications including oceanographic systems [4], multichip modules [5], large scale integrated circuits [6], power supply systems [7], avionics [8], and even passenger entertainment systems for the Boeing 767 [9] and the 777 [10].

The nature of BIT depends on the nature of the equipment which it monitors, as well as the scale of the system [2, 11]. System-wide BIT may be centralized, controlling all BIT functions, or may comprise a number of BIT centers (often at the line replaceable units), which communicate with each other and to a master processing unit which processes the results. A centralized BIT will often require dedicated hardware. BIT can also be incorporated and processed at the line replaceable units, to test the functionality of key circuits within a unit or on individual boards. The advantage of BIT at this level is to help identify problems closer to the root cause, and thus provide for cost-effective assembly and maintenance.

Two types of BIT concepts are employed in electronic systems, interruptive BIT (I-BIT) and continuous BIT (C-BIT). The concept of I-BIT is that normal equipment operation is suspended during BIT operation. Such BITs are typically initiated by the operator or during a power-up process. The concept of C-BIT is that equipment is monitored continuously and automatically without affecting normal operation. Periodic BIT (P-BIT) is an I-BIT which interrupts normal operation periodically in order to carry out a pseudocontinuous monitoring function.

BIT concepts are still being developed to reduce the occurrence of spurious failure indications [12] and to ensure operation of systems requiring high BIT availability [13]. New means for BIT implementation are also being developed [14, 15]. It has been pointed

out that the successful design and implementation of complex systems relies on a highly integrated team effort [16], and work has been conducted on developing means of carrying out concurrent design of test systems, along with the main system [17].

The reported benefits of BIT include shorter down times due to reduced fault finding time [3, 18], and fewer removals of operational units, resulting in reduced life cycle costs [18]. For go/no-go BITs, non-specialist operators are sufficient to carry our replacement to any subsystem level the BIT is designed for [3], and the BIT will indicate if a replacement or repair has been carried out properly.

Despite the apparent sophistication of BIT, there has been some concern that the requirement for BIT and the actual capabilities and limitations of the BIT have not been properly identified. For example, airline experience with modern avionics systems has indicated that spurious fault detection is unacceptably high. For example, the Airbus A 320, Lufthansa, had a daily average of 2000 error logs on the BIT. Around 70 of these corresponded with faults reported by pilots, while another 70 or so pilot reports of faults would have no corresponding BIT log. Of the 17 line replaceable units replaced every day, typically only two were found to have faults that correlated with the fault indicated with the reports. Thus even for commonly observed problems, fault detection is not complete, and fault isolation can be inaccurate [19, 20]. Another major problem in the design of BIT has been the failure to define the test requirements properly [20]. The persistence of such issues over the years is perhaps due to the fact that the use of BIT has been restricted to low volume systems, and because of the ubiquitous tendency to treat testing of systems as a low priority task.

This work looks at the broad objectives and implementation of BIT. The investigation is based upon our findings from highly accelerated life-cycle test (HALT) process carried out at the QualMark Corporation on an electronics board which was used as a seat-back module in commercial aircraft. The board included BIT which was used to diagnose the board for functional failures during testing. The principal findings of these tests with regard to the performance of the BIT are presented and discussed here. The implications of these findings to the concept of board-level BITs and system integration are also discussed along with conclusions as to cautions required in implementing BIT in electronic systems.

DEFINITIONS

Electronic equipment are generally designed to specifications, which include the range, or limits, of environmental and operating stresses, such as temperature, humidity, and vibration. This range is called the *specification limit.* The stress margin which is designed into the equipment, such that the equipment will function correctly beyond the specification limit, is called the *operational limit* for the equipment. Outside of the operational limit, the equipment may show failures due to performance-characteristic shifting (e.g., slew rate, voltage thresholds, and resistances) to an extent that the equipment no longer operates satisfactorily. If these failures disappear when the stress is decreased to values within the operational limit, they are termed *soft failures.* If the failures are irreversible, or *hard,* we term this to be the *destruct limit.* Fig. 1 shows the various limits and the associated failure types.

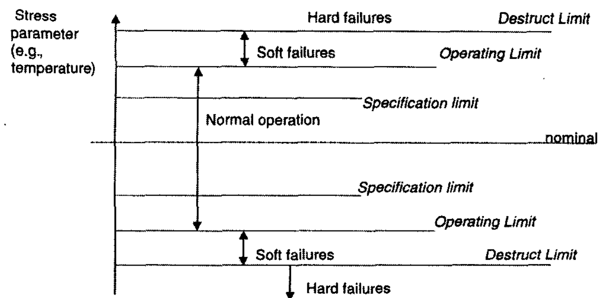

Fig. 1. Stress limits of electronic equipment.

EXPERIMENTAL WORK

Three seat-back processor electronics boards were subjected to HALT conditions at the Denver, CO facilities of QualMark corporation [21]. The boards were selected because they incorporate a comprehensive BIT, which we used for in-situ reliability monitoring of the board during testing.

Test-Bed

The test boards were seat-back processor modules (SPMs), which comprised the in-flight entertainment system for the Boeing 777. The system provides telecommunications, television, video, computer games, and other functions to the passenger via individual units located behind each seat. The SPM is a single-sided printed circuit board (PCB), of FR4 construction, with various microprocessors, memories, port and floppy disk controllers, inductors, capacitors, and resistors. The specifications for the board include operating temperatures from −10°C to +70°C, and shock loads up to 6 g for 11 ms.

The SPM BIT Equipment

The BIT equipment on the SPM, according to its documentation, is capable of identifying over 95% of all known faults [10]. The BIT is interruptive, in that it is usually initiated on power-up of the module.

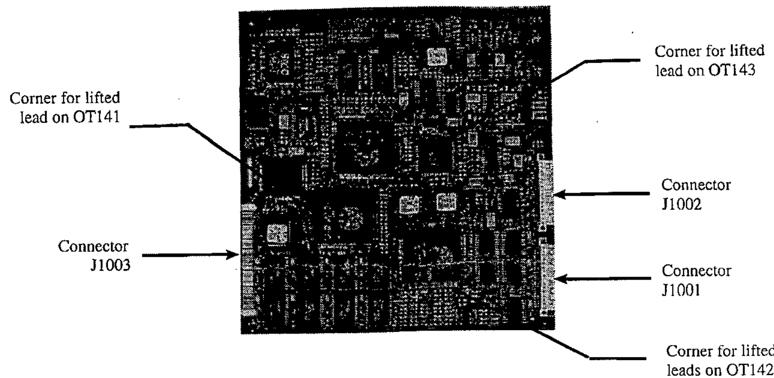

Fig. 2. Seat processor module, showing position of OTI ICs, leads lifted, and UART connector ports J1001, 1002, 1003.

The BIT performs a comprehensive range of self-tests, with each integrated circuit (IC) being subjected to at least one functional test. A *signal injection* technique is used, whereby a known input is "injected" at some point in the system and checking determines whether the correct outputs occur at other points in the system. The memory tests use an *incorporation of redundant information* technique, comprising cyclic redundancy checks (e.g., parity checks) and sum-checks.

The results from the BIT are provided to a serial port on the J1001 UART ribbon connector (Fig. 2) for ease of display and record. Each BIT test result is identified by a string of characters, such as 'VSEQ', or 'CPU', followed by '0' to indicate no failure detected, while any non-zero indicates that a particular test has failed and that a fault exists at the component indicated. For example, a failure at the CPU may be identified by the string 'CPU 1'.

Although interruptive in nature, the BIT was used as a periodic test by taking advantage of its watchdog reset capability, which resets the system and repeats all BIT if no external units are detected via the connector J1003. The BIT then cycles continuously, approximately every 10–15 s, throughout the duration of the accelerated stress tests.

Test Procedure and Results

The SPM boards were subjected to highly accelerated stresses, via the concept of HALT to determine the operating and destruct limits of the units. HALT testing may subject the test sample to stresses higher than those encountered in the field during shipping, storage, or operation. Because failure of the product during HALT cannot be precisely correlated to lifetime in the field, the rule of thumb is to continue to improve product performance under HALT as far as feasible. As commonly occurring failure mechanisms are accelerated under higher stresses, any improvement under HALT usually leads to improvement under fielded conditions [23].

Thermocouples and accelerometers were attached to each of the boards to record the stresses imposed during HALT. The BIT output was collected through an RS232 serial port for post-processing. Four HALT tests were carried out.

Temperature Step Stress (Sample 1): The test unit was subjected to cold thermal step stress tests beginning at 20°C, with the temperature decreasing in 10°C increments at 20 min intervals. The temperature was lowered to −100°C. At this time cold testing was interrupted, and hot step testing was carried out. Hot thermal step stress testing began at a set-point temperature of +20°C with the temperature increasing in 10°C increments at 20 min intervals. The dwell time was reduced to 15 min above 70°C, and reduced to 10 min above 100°C.

1) No cold temperature failures were observed.
2) A EPROM_CS error occurred repeatedly at each test cycle at or above 100°C.
3) Five components associated with the video component OTI_43 failed twice at or above 110°C.
4) A PIC/NMI error occurred repeatedly at or above 130°C.
5) TIMER_0 and TIMER_1 errors occurred at or above 135°C.
6) The serial port was intermittent at or above 140°C. The displayed BIT data on the screen was corrupted and the system locked-up.

Rapid Thermal Transitions (Sample 1): The device under test was subjected to five rapid temperature cycles from −100°C to +130°C at an average thermal transition rate of 60°C/min using 10 min dwells at each temperature set-point. The thermal transition rate is an average rate computed from an average of all the temperature data points collected during testing. Air temperature limits were set to −105°C and +140°C to prevent excessive overshoot. The key

results were:

1) The five components associated with the video component OTI_43, that were observed to fail at 110°C during the thermal step test, failed on every test cycle at approximately 120°C during rapid thermal transitions.

2) Upon completion of five cycles, a visual inspection revealed that the conformal coating had flaked off several components. This may have occurred earlier and gone unnoticed.

Vibration Step Stress (Sample 2): The device under test was subjected to vibration step stress beginning at a set-point of 5 Grms with the vibration increasing at 10 min intervals. Vibration load levels were chosen to match values for which theoretical predictions for solder joint fatigue had been calculated beforehand. Testing was continued up to 58 Grms. The bandwidth for all measurements was 0 to 3 kHz. The key results were:

1) The connectors J1001 and J1002 on test sample 2 backed out slightly at 36 Grms.

2) The sample had a OTI_42 error 813 s into the dwell at 55 Grms.

3) A REFRESH error occurred 1311 s into the dwell at 55 Grms.

Combined Environment (Sample 1, 2, 3): The test unit was subjected to temperature cycles from −100°C to +130°C at an average transition rate of 60°C per min, combined with vibration. Due to numerous failures observed, the upper limit for sample 2 was reduced to 105°C for the second thermal cycle. Testing for sample 3 was started at an upper limit of 105°C, which was then reduced to 90°C. The vibration began at a set-point of 10 Grms and was increased in 10 Grms increments at the end of each thermal cycle. The dwell at each temperature extreme was 10 min. This was continued to 58 Grms, which was the maximum value for which theoretical estimates could be obtained. The key results were.

1) The unit lost serial communications at 100°C and 30 Grms. For samples 1 and 3, the BIT was transmitting random corrupted characters. The temperature was reduced to 50°C and it was still failing, but it recovered at 25°C.

2) The serial communications stopped functioning after several cycles of exposure to −100°C to 140°C cycles and 58 Grms.

Principal Findings

Operating Limit Detected by BIT: The lower operating limit was not reached by −100°C, the minimum temperature for our tests, and thus, could not be determined. The BIT proved extremely consistent in determining the upper operating temperature limit of the SPM. Around 100°C, a failure at the EPROM ('EPROM_CS 1') was observed on all three boards tested, and more importantly, for each board, a few degrees drop in temperature followed by a dwell of 20 to 30 s resulted in a "re-test OK" BIT report, indicating soft failure. As the temperature was increased to 130°C, the programmable interrupt controller ('PIC/NMI 1') began to fail. This was also a soft failure, and disappeared when the temperature was lowered a few degrees. The timers ('TMR_0 1' and 'TMR_1 1') began to fail at 135°C. No further errors could be determined. This finding is of particular importance to the occurrence of could-not duplicate (CND) failures, and is the subject of an associated paper [22].

Operating Limit of the BIT: Above 120°C the serial data from the BIT began to corrupt with approximately one character in twenty being incorrect or missing. This grew steadily worse as the temperature was increased until finally at 140°C, the BIT stopped transmitting data. After decreasing the temperature, the BIT recommenced transmission indicating the BIT failure to be soft. This finding is of particular importance to the occurrence of CND failures, and is the subject of an associated paper [22]. Above 140°C the ribbon connectors started to melt. It was therefore assumed that the operating limit of the BIT was somewhere between 120°C and 140°C, depending on the desired clarity of the data stream.

Operating Limit Drift with Stress History: Following combined temperature cycling and omni-axial vibration at 30 Grms, the upper temperature limit of operation of the board was observed to decrease. The same order of failures (EPROM, PIC/NMI, TMR_0, TMR_1) were observed but at correspondingly lower temperatures, thus suggesting the presence of accumulated damage. It should also be noted that the BIT operating limit also decreased.

False Reports Attributed to Connector Failure: During the vibration step stress test of one of the samples, the BIT detected multiple failures across most of the ICs on the board. These errors occurred at vibration levels as low as 10 G rms. The initial assumption was that the SPM was prone to vibration-induced failure. However on verifying the connections, the J1001 ribbon connection was found to have worked loose. The connector was reseated and secured with Kapton tape, and the vibration testing was repeated [21, sect. 5.1.3]. No failures were observed at any step stress up to 17 min at 58 Grms except for a single, nonrepeated OTI42 failure.

BIT Response to Lead Lifting: To determine the extent of BIT coverage, leads from various packages were lifted off the board. The larger flat packs, OTI41, 42, and 43 provided suitable subjects due to the ease of removing the relatively large gull-wing leads. The corner lead was lifted as shown on OTI41 (A).

The subsequent BIT reports consistently indicated an *initialization* failure and a fault on the DMA. Following resolder, both faults disappeared. However, the corner leads were also lifted on OTI42 and OTI43 (B and C). Neither resulted in a BIT failure report of any kind. Further, eight adjacent leads were lifted from the lower left-hand corner of OTI42 (D). Again no failures were reported on subsequent power-up, by the BIT. Only after the ninth lead was detached were failures reported. It was concluded that the BIT doesn't have complete coverage.

DISCUSSION

The suitability and effectiveness of BIT must be judged in terms of its ability to meet the desired objectives. The relevant findings with regard to the common modes of failures versus the failure types detected by the BIT, the correctness of BIT results, as to the location and type of actual failure versus the failure indicated, as well as the possible impact of extraneous considerations like improper connector seating on the results output by the BIT are discussed below.

Detection of CND Failures

The "soft" failures that occurred can be responsible for CND failures in the field, due to the inability to reproduce the field environment responsible [22]. The SPM BIT proved useful for identifying the nature of such failures under HALT but these failures could not be detected by this system in the field, unless BIT was implemented as continuous instead of being run once only on system power-up.

Failure Location

Determination of the location of failure can be a problem because an open circuited interconnection can be considered to be at the output of one unit or at the input of another. In the case of solder joint fatigue at a particular component, identification of the responsible component is not evident. For example, when the ninth lead lifted on the OTI42 flat pack, the flat pack OTI41 was identified as having failed. In actuality neither component failed [1].

CONCLUSIONS

BIT is defined as an on-board means to identify and locate faults, and over the last decade, has become an established means of providing diagnostic support. When used for in-situ monitoring of the board, we found that BIT indicated a number of transient and soft failures which would have been classified as CND in a post-failure analysis. The BIT also provided evidence of operating limit drift for boards subjected to high temperature and vibration loads. However while the indication of a fault by a BIT might aid in detection of failure, the actual site and mechanism of failure cannot always be determined accurately enough to always make intelligent maintenance decisions, especially if the coverage is incomplete. For example, the proportion of artificially induced hard failures remained undetected and some failures that were indicated were diagnosed as having occurred at the wrong location. The BIT also gave false component failure reports when the edge connector at the board became unseated. Such reports in the field can lead to unnecessary replacements.

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Manu Dube obtained his B.Tech. in mechanical engineering from the Indian Institute of Technology, Bombay and MSME (design) from the State University of New York at Binghampton. He is currently a research assistant and doctoral student at CALCE, University of Maryland. His interests include physics of failure-based reliability monitoring of electronic systems and physics-based modeling of electronics assembly processes. He is a student member of the ASME and IMPAS.

Marjorie Ann Natishan is Assistant Professor in the Mechanical Engineering Department of the University of Maryland. She received her Ph.D. from the University of Virginia in materials science in 1989. Prior to joining the faculty at Maryland, she worked for 11 years in the Carderock Division of the U.S. Naval Surface Warfare Center on research including micromechanisms of fracture in metals, metallurgical factors affecting strength, toughness and weldability of high-strength steels and test methodology for assessment of dynamic fracture analyses. She is currently working on processing effects on solder joint reliability for high-temperature applications, micro-electronics health monitoring and assessing materials issues in power electronics applications for the Next Generation Vehicles Program for the U.S. DOE. She is chairman of the Society for Machinery Prevention Technology and has authored over 40 publications and reports.

Reg Williams is a project officer in the Directorate of Sensors and Electronic Systems at Abbey Wood. He graduated B.Eng. in electrical and communications engineering at the University of Bristol in 1996. This paper was written during a Visiting Scholarship at CALCE-EPRC.

Julian Banner was also a Visiting Scholar at CALCE-EPRC. He graduated M.Eng. in electronic engineering at the University of Nottingham in 1996 and is now a project officer in the Directorate General of Submarines at Abbey Wood.

Ian Knowles is Principal R&M Engineer in the Directorate of Procurement Management Policy at Abbey Wood. He served as an engineering apprenticeship with the De Havilland Aircraft Company and graduated B.Sc. in mechanical engineering from London University in 1963 and M.Sc. in quality and reliability engineering from the University of Birmingham in 1973. He is a Chartered Mechanical Engineer and his career has included positions in engineering design, project manager and quality assurance in both industry and the civil service. He is chairman of the Engineering Working Group responsible for the drafting of UK R&M Engineering Defense Standards.

Michael Pecht is the Director of the CALCE Electronic Products ,md Systems Center at the University of Maryland and a Full Professor. Dr. Pecht has a M.S. in electrical engineering and a M.S. and Ph.D. in engineering mechanics from the University of Wisconsin at Madison. He is a Professional Engineer, an IEEE Fellow, an ASME Fellow, and a Westinghouse Fellow. He has written eleven books on electronics products development. He served as chief editor of the IEEE Transactions on Reliability for eight years and on the advisory board of IEEE Spectrum. He is currently the chief editor for Microelectronics Reliability from Elsevier Publications. He serves as a consultant for various companies, providing expertise in strategic planning, design, test, and risk assessment of electronic products and systems.