Prognostics implementation of electronics under vibration loading

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Abstract

In this paper, a methodology is developed for monitoring, recording, and analyzing the life-cycle vibration loads for remaining-life prognostics of electronics. The responses of printed circuit boards to vibration loading in terms of bending curvature are monitored using strain gauges. An analytical model calibrated by finite element analysis is developed to calculate the strain at interconnects using the measured response. The interconnect strain values are then used in a vibration failure fatigue model for damage assessment. Damage estimates are accumulated using Miner’s rule after every mission and then used to predict the life consumed and remaining-life. The methodology has been demonstrated for remaining-life prognostics of a printed circuit board. The result has also been verified by the real-time to failure of the components by checking the components’ resistance data.

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1. Introduction

Prognostics is a method that permits the assessment of the reliability of a system under its actual application conditions. It integrates sensor data with models that enable in-situ assessment of the deviation or degradation of a product from an expected normal operating condition (i.e., the system’s “health”) and also predict the future state of reliability based on current and historic conditions. Prognostics for electronics has just been developed in recent years. Vichare and Pecht [1] have summarized the main approaches to implementing prognostics into electronics. However, this has not been significantly focused on prognostics of electronics with respect to vibration loading.

During the life-cycle of an electronic product, it will be subject to various complex loadings, including vibration. These loads can be monitored in-situ and used in conjunction with physics-based models to assess their impact on the health of the components, interconnects, assemblies, and enclosures of the unit. Information about ongoing health provides advance warning of failure, enables condition-based maintenance, and reduces life-cycle costs.

Mishra et al. [3] introduced the life consumption monitoring (LCM) methodology, which combined in-situ measured vibration loads with physics-based stress and damage models for assessing the life consumed. The application of the LCM methodology to the prognosis of electronics was illustrated with two case studies [2,3]. The test vehicle consisted of an electronic component-board assembly placed under the hood of an automobile and subjected to normal driving conditions in the Washington, DC, area. The test board incorporated eight surface-mount leadless inductors soldered onto an FR-4 substrate using eutectic tin–lead solder. Solder joint fatigue was identified as the dominant failure mechanism. Vibrations were measured in-situ on the board in the application environment. Using the monitored environmental data, stress and damage models were developed and used to estimate consumed life. The LCM methodology accurately predicted remaining-life.

Mathew et al. [4] applied the LCM methodology in conducting a prognostic remaining-life assessment of circuit cards inside the space shuttle solid rocket booster (SRB). The vibration time history recorded on the SRB from the pre-launch stage to splashdown was used in conjunction
with physics-based models to assess the damage caused due to vibration and shock loads. Using the entire life-cycle loading profile of the SRBs, the remaining life of the components and structures on the circuit cards were predicted. It was determined that an electrical failure was not expected within another forty missions. However, vibration and shock analysis exposed an unexpected failure of the circuit card due to a broken aluminum bracket mounted on the circuit card. Damage accumulation analysis is determined that the aluminum brackets had lost significant life due to shock loading.

The above studies were based on the frequency domain and relied on software (calcPWA\(^1\)) to perform prognostics. Although the reliability predictions are easy to execute, they are large and cannot be integrated directly into the microprocessor.

The prognostics approach developed in this paper is based on the time domain and analytical method. Because of its small computational size, this method can be easily incorporated into the hardware for real-time calculation.

2. Prognostics method for electronics in the vibration loading environment

Field failures related to the operating environments of electronic equipment show that about 55% of the failures are due to high temperatures and temperature cycling, twenty percent are related to vibration and shock, and another twenty percent are due to humidity [6]. Prognostics methods for electronics under thermal loading have been summarized by Vichare and Pecht [5]. This paper will address the prognostics methods for electronics under vibration loading. Therefore, the experiments were designed to make vibration the dominant factor.

The overall approach of prognostics for electronics under vibration loading is shown in Fig. 1. In this approach, we focused on solder joint failure, since it is critical and the weakest link of electronics under vibration. First, we can use a virtual qualification tool, such as calcPWA software, to quickly assess the printed circuit board (PCB) assembly. Since some complicated PCBs have hundreds of components, we need to identify those most likely to fail. The result shows that solder joint vibration fatigue failure is indeed the dominant failure model. The software also identifies the natural frequency of the PCB, the PCB response (bending curvature), and the locations of critical components at certain vibration loading levels. This allows placing sensors at those areas to monitor the local PCB response. In this study, we put the strain gauges at the back of PCB centered underneath the critical components.

Then we built the database. The database is a relationship between PCB strain and solder strain. (We will give details on how to build this relationship below.) From the measured PCB strain and database, we can calculate the solder strain, then use a cycle-counting algorithm to extract the load feature. This is put into the failure fatigue model to calculate the damage. Miner’s rule is used to calculate the accumulated damage. Based on that number, we can predict the remaining life of the component.

2.1. Characterization of the test board

The board used for demonstrating the prognostics approach is shown in Fig. 2. It has six ball grid array (BGA) components and six quad flat package (QFP) components. For each BGA, it has four daisy chains, and for each QFP, it has one daisy chain. All components are mounted on one side of PCB.

The calcPWA software was used to calculate the natural frequency of the board, and the results were compared to experimental results (see Table 1). The largest displacement occurred in the middle of the board and was found

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\(^1\) calcPWA is a virtual qualification tool developed by CALCE, University of Maryland, College Park.
to be proportional to the stress level of the interconnect. This is also in accord with Steinberg’s model [6].

2.2. Database from PCB strain to solder strain

While solder strain is the factor of interest, we cannot measure it directly. On the other hand, PCB strain can be easily measured using strain gauges attached to the PCB. Therefore, we need to establish the relationship between PCB strain and solder strain.

First, we built the local finite element analysis (FEA) model to obtain the strain in the corner solder joint and the strain on the back side of the PCB during bending, as shown in Fig. 3. The corner solder joint is more critical one than any other joints in the FEA results, including the joint underneath the corner of the die. Secondly, we plotted the relationship of PCB strain and solder strain, and used a linear curve to fit it (Fig. 4). The purpose of using a linear relationship was to calibrate the analytical approach later.

The analytical approach we used is based on Chen’s model [7]. The assumption of this approach is that the local PCB bending curvature remains constant. The 2D model for a ball grid array (BGA) component is shown in Fig. 5.

The following equations (1)–(6) were used to calculate the solder strain from the PCB strain:

\[ k = \frac{1}{R} = \frac{\varepsilon_{PCB}}{t_{PCB}/2} \]

\[ Z_i = \sqrt{R^2 - \left(\frac{L}{2} - x_i\right)^2} - \sqrt{R^2 - \frac{L^2}{4}} \]

\[ \delta_0 = \frac{1}{m} \sum_{i=1}^{m} Z_i \]

\[ \delta_i = \delta_0 - z_i \]

\[ \varepsilon_{solder} = \frac{1}{\alpha} \frac{\delta_i}{H_{solder}} \]

\[ \alpha = f(E_{solder}, D_{solder}, N_{solder}) \]

where \( R \) is curvature radius, \( t \) is PCB thickness, \( H \) is solder height, \( K \) is curvature, \( L \) is component length, \( x \) and \( z \) are the locations of each component in special directions, \( \delta \) is displacement of solder joint, \( \varepsilon \) is strain, and \( \alpha \) is the
interconnect factor. \( E \) is the solder’s Young’s modulus, \( D \) is solder ball maximum diameter, and \( N \) is the number of solder balls on one edge. For BGA components, the interconnect factor is the function of the solder’s Young’s modulus, solder ball diameter, and number of solder balls on the edge suffering the largest PCB bending curvature. Solder ball height is not included in the interconnect factor, since it has already been accounted for in Eq. (5).

For a 3D problem with full grid array (Fig. 6), we can use Eqs. (7)–(14). When the boundary along \( Y \) directions has been clamped, \( R_y \) will be infinite, and \( Z_{ij} \) will be 0, so the problem will revert to the 2D problem again.

\[
\frac{1}{R_x} = \frac{\varepsilon_{PCB-x}}{t_{PCB}/2}, \quad \frac{1}{R_y} = \frac{\varepsilon_{PCB-y}}{t_{PCB}/2},
\]

\[
Z_{il} = \sqrt{R_x^2 - \left( x_i - \frac{L_x}{2} \right)^2} - \sqrt{R_x^2 - \frac{L_x^2}{4}},
\]

\[
Z_{ij} = \sqrt{R_y^2 - \left( x_j - \frac{L_y}{2} \right)^2} - \sqrt{R_y^2 - \frac{L_y^2}{4}}.
\]

\[
X, Y, Z
\]

Fig. 6. 3D analytical model for full grid array.

For the interconnect factor \( \chi \), we assume that \( E, D, \) and \( N \) are independent. As long as the solder ball diameter is less than the solder pitch, the number of solder balls along one edge of the component will not be constrained. Series of FEA analyses were carried out to evaluate the effect of \( E, D, \) and \( N \) (Fig. 7). By evaluating or changing one parameter at a time, leaving the other two parameters the same, we could ascertain how the parameter contributed to the solder strain and PCB strain relation. We repeated this three times, determining the effects of all three parameters.

For example, in Fig. 7, the \( X \) axis represents the change in the parameters, and the \( Y \) axis shows the nominal value of the solder strain and PCB strain relation. The power line curve was used to represent the parameter effect. Then we used BGA169 as a base line to compare the analytical approach with the FEA result (linear curve fit relation), and got the final interconnect factor shown in Eq. (15).

\[
\varepsilon_{solder} = \frac{1}{3.83 \left( D_{solder} / 0.76 \right)^{2.67} \left( K_{solder} / 29914 \right)^{0.28} \left( N_{solder} / 13 \right)^{2.63}} \frac{\delta_i}{H_{solder}}.
\]

We then used the interconnect factor to calculate the relationship between PCB strain and solder strain for BGA225 and BGA352. The analytical approach results were compared with the FEA results shown in Table 2.

For a 3D problem with peripheral array (Fig. 8), such as QFP components, Eqs. (16)–(21) were used to calculate the corner interconnect displacement. We could not calculate the solder strain directly, since it was a gull-wing lead, so we calculated the gull-wing stiffness in \( Z \) direction. This could be calculated from Eq. (22), which is a simplified equation from Kotlowitz’s model [8] when only consider the stiffness in \( Z \) direction. From the interconnect displacement and the lead stiffness, we calculated the force in the
gull-wing lead, which should be the same as the force in the solder in $Z$ direction. Dividing the solder force by the solder bond area provided the solder stress, which can be transferred to the solder strain using a material strain and stress curve.

$$
1 \frac{Rx}{\varepsilon_{PCB}} = \frac{e_{PCB}}{C0} \times \frac{t_{PCB}}{2}; \\
1 \frac{Ry}{\varepsilon_{PCB}} = \frac{e_{PCB}}{C0} \times \frac{t_{PCB}}{2}; \\
Zi = \sqrt{Rx^2 - \left( \frac{x_i - L_1}{2} \right)^2} - \sqrt{Ry^2 - \frac{L_2^2}{4}}, \\
Zj = \sqrt{Rx^2 - \left( \frac{x_j - L_1}{2} \right)^2} - \sqrt{Ry^2 - \frac{L_2^2}{4}}, \\
\delta_0 = \frac{1}{m + n} \left( \sum_{j=1}^{n} Z_{ij} \right), \\
\delta_{ij} = \delta_0 - z_{ij}, \\
SIZ = \frac{wEt^3}{L_1^2 + \frac{4L_1^2}{3} + 2.4(1 + v)L_2^2},
$$

where $\varepsilon$ is the interconnect factor, $A$ is the solder bond area, and $f$ is the strain and stress relation curve for that material. The interconnect factor was calibrated by FEA results using the same approach as shown for BGA component calibration.

3. Equipment setup and process

3.1. Vibration shaker setup

The test board was mounted on a vibration shaker using a two-edge clamped boundary condition, as shown in Fig. 9. The shaker could excite vibration in the out-of-plane direction. The step stress test shown in Table 3 was then conducted in four steps lasting a total of 21 h. In each step the loading condition was random vibration loading with frequency response from 40 Hz to 500 Hz. Fig. 10 shows the input profile that generated the random vibration loading. Prior to the step stress test, we used one board to carry out initial tests, such as natural frequency analysis. From these, we knew the strain along the length of the PCB was much higher than the strain along its width. Therefore,
the latter could be neglected in the test. We also analyzed the noise of the sensor under a no-loading condition. The strain range within the noise level was filtered out during the cyclic counting of the step stress monitoring data, since it would not factor into the damage calculation.

3.2. Sensor location and data acquisition setup

The strain gauges were mounted on the back side of the PCB (Fig. 11). Strain data were collected by the NI SCXI1314 data acquisition card incorporating the Labview program. The program was coded for both the time triggered and signal triggered functions. In time trigger mode, the program could record one thousand data (in 1 s) every minute. In the signal trigger mode, the program could record one thousand data which including 5% pre-trigger data (in 1 s) when the signal met the threshold. The threshold was set at ninety percent of the maximum value in the initial test. The time trigger function was used to capture the loading distribution, while the signal trigger function was used to catch the abnormal stress condition during a gap in the time trigger function, such as sudden shock.

3.3. Resistance measurement

Resistance of each component was measured through a daisy chain that connects to the data logger. The data logger monitored the resistance in-situ. The failure criteria in this test was defined as follows: The daisy chain resistance is over 50 Ω (first spike), and it repeats similar behavior nine more times in the next ten percent of the time to the first spike. In this case, the first spike is considered the time-to-failure point for the component. For the conservatism purposes, we chose 50 Ω rather than the 300 Ω mentioned in the IPC standard [9]. For multiple daisy chains in one component, we consider the first daisy chain failure time as the component failure time.

4. Damage calculation and remaining life prediction

The strain measured on the PCB could be transferred to the solder strain using the relation built in the previous paragraph. Cycle-counting for the solder strain extracted the load feature – strain range. The strain noise was filtered out during the cycle-counting algorithm. Then binning the strain range (Fig. 12) was done. The bin width was selected using an optimal bin width [10] (Eq. (25)).

$$h_{\text{opt}} = 1.06\bar{s}n^{-1/5},$$

(25)

where $h$ is the bin width, $s$ is the estimate of standard deviation, and $n$ is the sample size. The binned strain ranges were put into the failure fatigue model (Eq. (26)) to obtain the time to failure for each strain range level. Miner’s rule was then used to assess the accumulated damage (Eq. (27)). Damage was defined as the extent of a part or product’s degradation or deviation from its normal operating state. The aim of damage assessment is to convert the number of cycles-to-failure values obtained from the physics-of-failure analysis into a metric for life consumption:

$$\Delta e = c(N_i)^n,$$

(26)

$$D_{\text{total}} = \sum_{i=1}^{s} \frac{n_i}{N_i},$$

(27)

where $\Delta e$ is the strain range, and $c$ and $n$ are the material constants. The damage fraction ($D$) at any stress level is linearly proportional to the ratio of the number of cycles of operation ($n_i$) to the total number of cycles that would produce failure ($N_i$) at that stress level. When $D > 1$, the failure is considered to have occurred. We accumulated damage...
for each hour, and then calculated the remaining life at each hour by Eq. (28):

$$RL_N = \frac{N}{DR_N} - N$$  \hspace{1cm} (28)

where $RL_N$ is the remaining life at the end of $N$th hour, and $DR_N$ is the damage ratio accumulated at the $N$th hour. The history of accumulated damage and the remaining life prediction for component BGA352-1 are shown in Figs. 13 and 14. From Fig. 14, we see that the predicted remaining life was constantly changing. One reason is that the useful life was being consumed every hour; the other is that the loading condition was also changing. So, the data in the first few hours could not accurately predict the remaining life unless the loading condition remained the same. This explains why in-situ monitoring was necessary.

From Fig. 14, the prognostics approach appeared able to predict a remaining life that matched the experimental results. A summary of other component predictions is presented in Table 4. (NA in the table means there is no strain gauge at the back side of PCB, local strain cannot be used for the prediction.) We can see that the results for some components match quite well; while others differ widely. However, the overall trends still match.

5. Discussion

This paper demonstrated the physics-of-failure approach to implementing the prognostics of electronics under vibration loading by monitoring the loading condition. From Table 4, we see that the prediction for some components matches very well with the experimental results. Four prediction results were within ten percent discrepancy. Only one prediction produced an error over 100%. The overall prediction trend appears valid. One possible explanation of the discrepancy is the uncertainty of the input material properties and fatigue constant. Therefore, future investigation will focus on integrating the uncertainty analysis into the current prognostics approach.

6. Conclusions

This paper presents the development and demonstration of the prognostics methodology for electronics under vibration loading. By monitoring, recording, and analyzing the life-cycle vibration loads of printed circuit boards, the remaining life of electronic components can be assessed. The responses of printed circuit boards to vibration loading in terms of bending curvature are monitored using strain gauges. An analytical model calibrated by finite element analysis was developed to calculate the strain at interconnects using a measured response. This approach enables the calculation of interconnect damage accumulation and
prognostics assessment when using strain gauges measuring the board response.

References