SUMMARY & CONCLUSIONS

This paper describes an assessment of the remaining life of solder interconnects for 13 different insertion mount packages used in an engine control electronics. The assessment consisted of using simulation to determine the mean time to failure of solder joint interconnects between the package leads and printed wiring boards under applied temperature cycle conditions. The simulation results were confirmed by accelerated testing for a 132-Pin Grid Array (PGA) and field data for a 40-lead side-brazed Dual In line Package (DIP). Loading conditions include an accelerated test condition of $-45^\circ$ to $100^\circ$C and a service loading condition of $10^\circ$ to $75^\circ$C with an extended dwell at $60^\circ$C. Predicted mean interconnect life expectancy ranged from 4,000 in the worst case to 130,000 cycles. Results indicate a brazed leaded ceramic dual inline package with 40 leads is likely to fail first and a 2 lead plastic encapsulated axial capacitor is the least likely to fail. The early failure of the 40-lead side-brazed DIP was confirmed by the service performance data. The service life remaining after failure of the 40-lead side-brazed DIP was estimated to be 7,800 cycles.

2. INTRODUCTION

The cost of product ownership in addition to acquisition cost is a strong function of the sustainment costs associated with fielding and maintaining an electronic system [Ref. 1]. Avionic equipment usually have operational lifespan of over 20 years. During this lifespan many elements of an electronic equipment structure will degrade. If any approach the point of failure, a strategy for their replacement or refreshing during their life may be needed. In order to reduce the cost associated with fielding and maintaining of electronic system, an avionics equipment supplier must have an understanding of the life expectancy of the electronic system and must be assured that the electronic system can meet the necessary life cycle requirements.

Remaining life assessment provides information about the ability of a device and the interconnections made to the device to meet the device required performance specifications in its life cycle application environment for the remaining service life of the product. Traditionally, wear out life has not been a consideration and a constant assigned failure rate obtained from weighted factors has been assumed. This traditional approach includes no understanding of the behavior of materials and structures and the wear out mechanisms that may impact the service life.

For a remaining life assessment to be successful, it will require a methodology with the capability of modeling multiple failure mechanisms and the capacity for running multiple stress conditions. A good remaining life assessment methodology should cover the underlying quantitative and qualitative relationship between the major parameters of the object investigated in a set of mathematical equations with relevant boundary conditions. The ultimate goal of any life assessment methodology is to reveal relatively complicated relationships that exist but are hidden behind the physics of the object.

The remaining life assessment presented in this paper is based on the scientific determination of the dominant failure mechanisms and failure sites within the electronic component assemblies by characterizing the stresses in the system using thermal analyses as inputs for analytical models derived from fundamental physical phenomena. The failure mechanism of primary concern in this study is fatigue damage to insertion mount solder joint reliability caused by cyclic thermal loading.

3. SIMULATION APPROACH

The reliability of the solder joint attachment of electronic components mounted to circuit board substrates requires particular attention during use. Thermal expansion differences in material as well as temperature changes due to internal power dissipation of the components in combination with system internal or external temperature variations can damage the package to board interconnection (i.e., solder joints and package leads) [Ref. 2]. During operation, solder joints and package leads can be

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1 Caused by component or system load fluctuation or on/off cycles, by diurnal cycles, or by seasonal changes caused by component or system load fluctuation or on/off cycles, by diurnal cycles, or by seasonal changes
subjected to considerable cyclic strains caused by dissimilar thermo-mechanical properties of: the component packages, the substrates to which they are soldered, the solder and the lead material and configuration.

Life assessment of solder joints is often made by performing: a macro-analysis of the entire assembly to identify the critical joint and the magnitudes of its end deformation (end displacements and rotations) and a micro-analysis of the isolated critical joint with boundary conditions obtained from the macro-analysis [Ref. 3]. The results from the microanalysis (stresses, strains, energies, etc.) are used to estimate solder joint life with the help of a fatigue law. In general, analytical models are widely used to predict reliability, which have a power law structure [Ref. 4]:

\[
CTF = C \cdot (S)^n
\]

where CTF is cycles-to-failure, \( C \) is a constant that depends on specific materials and product parameters, \( S \) is a stress metric, and \( n \) a material parameter. This equation provides an approach for predicting interconnect failure. Most of the technical content for the analytical models are included in the technical references rather than in this paper [Refs.5, 6].

4. INSERTION MOUNT PACKAGES

In this study, insertion mount interconnects found in electronic assemblies designed by TRW are examined. The electronic assemblies are part of an engine mounted control unit, which has been in service for nearly 15 years. A representative assembly is depicted in Figure 1. The assembly consists of electronic components inserted in an eight-layer, 2.26 mm thick, FR4 laminate with a 0.7 mm aluminium heat plane.

Table 1: Packages characteristics

<table>
<thead>
<tr>
<th>Package</th>
<th>Case Material</th>
<th>Lead Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>40 CDIP</td>
<td>Ceramic</td>
<td>Side Brazed</td>
</tr>
<tr>
<td>132-CPGA</td>
<td>Ceramic</td>
<td>Pin</td>
</tr>
<tr>
<td>28 CDIP</td>
<td>Ceramic</td>
<td>Regular</td>
</tr>
<tr>
<td>24 DIP wide</td>
<td>Ceramic</td>
<td>Regular</td>
</tr>
<tr>
<td>24 DIP</td>
<td>Ceramic</td>
<td>Regular</td>
</tr>
<tr>
<td>20 DIP</td>
<td>Ceramic</td>
<td>Regular</td>
</tr>
<tr>
<td>10 Single Inline Package (SIP)</td>
<td>Plastic</td>
<td>Regular</td>
</tr>
<tr>
<td>18 DIP</td>
<td>Ceramic</td>
<td>Regular</td>
</tr>
<tr>
<td>20 brazed DIP</td>
<td>Ceramic</td>
<td>Side Brazed</td>
</tr>
<tr>
<td>18 brazed DIP</td>
<td>Ceramic</td>
<td>Side Brazed</td>
</tr>
<tr>
<td>16 brazed DIP</td>
<td>Ceramic</td>
<td>Side Brazed</td>
</tr>
<tr>
<td>14 brazed DIP</td>
<td>Ceramic</td>
<td>Side Brazed</td>
</tr>
<tr>
<td>2 PDIP</td>
<td>Plastic</td>
<td>Regular</td>
</tr>
</tbody>
</table>

Table 2 presents a summary of the material properties used in the analysis. Engineering judgment was required in assigning lead geometry and package coefficient of temperature expansion (CTE).

Table 2: Properties for different materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Description</th>
<th>E (GPa)</th>
<th>CTE ( 1/\degree C \times 10^{-6} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kovar (Fe-Ni-Co)</td>
<td>Leads</td>
<td>138</td>
<td>5.9</td>
</tr>
<tr>
<td>Ceramic</td>
<td>Package</td>
<td>130.1</td>
<td>6</td>
</tr>
<tr>
<td>FR-4</td>
<td>Board</td>
<td>17.2</td>
<td>19</td>
</tr>
<tr>
<td>Solder</td>
<td>Eutectic</td>
<td>10</td>
<td>21</td>
</tr>
<tr>
<td>Plastic (2 leaded DIP and 10 leaded resistor network only)</td>
<td>Package</td>
<td>15.6</td>
<td>25</td>
</tr>
</tbody>
</table>

The interconnect geometries for the soldered package are depicted in Figure 2. Input values for the lead geometry were approximated by examining the relevant dimensions from part data sheets.
5. LIFE CYCLE LOADING PROFILE

The reliability of a part/system is dependent on life cycle loads, which are experienced by the part/system including manufacturing, assembly, storage, transportation, rework, and field use. These loads may be grouped into two types – environmental loads, which the part/system experiences due to the external surroundings, and operational loads that arise as a result of the functional operation of the part/system itself. Examples of environmental loads include ambient temperature, humidity, mechanical forces, pressure, acoustic and vibration loads. Operational loads include current and voltage. It is important to note that in addition to load magnitudes, the load rates, load range, and the duration of load are also important.

The product data used in this study is from a mature design where the operational electrical loads and the manufacturing and transport stresses to which the boards were subjected are well understood and the issue in question is the wear out life of the solder interconnects under extended thermal cycling, primarily due to temperature changes during aircraft operation. Internal heating accounts for a maximum of 10 °C in an average cycle range of up to 65 °C.

The typical service temperature cycling condition for the assembly is depicted in Figure 3. The cycle was approximated as having a maximum dwell temperature of 67.5 °C. The ramp rates were taken to be 10 minutes with dwell times of 130 minutes.

6. ANALYSIS AND DISCUSSION

The time to failure of the solder interconnects for the packages was evaluated using a mathematical model to approximate the stress and strain history for a specific interconnect assembly under a specific loading condition. The approximated stress history was subsequently used as input to a material damage law to forecast cycles to failure. The inputs for the model are broken into package (body) parameters, interconnect dimensions, attach parameters, solder parameters, and stress condition parameters.

The strain range produced in the solder joint due to the thermal expansion mismatch between the package body and the board and the local thermal expansion mismatch between the lead and board are considered. The strain is assumed to have sufficient time to completely relax. The time to failure is calculated using a Manson Coffin (power law) relationship between the cycles to failure and the inelastic strain range.

5.1. Estimated Life under Test Condition

Failure assessment results from the application of the previously mentioned failure models for the selected packages under a qualification test condition of –45 °C to 100 °C with 15 minutes dwells and ramps are provided in Figure 4. Figure 4 shows a range of cycles to failure from 1,430 cycles for the 40-lead side-brazed DIP to 30,400 for the two lead plastic encapsulated capacitor.

Failure assessment results from the qualification testing gave a cycles to failure for the 132 lead ceramic pin grid array (PGA132) of approximately 4,000 cycles. The simulation prediction for the PGA132 was approximately 2,810 cycles for the applied qualification profile.

![Figure 3: Typical aerospace flight cycle](image)

![Figure 4: Life assessment for different packaging arrangements](image)
5.2. Estimated Life under Service Condition

In addition to the test condition, the packages were examined under the service condition depicted in Figure 3. The assessed cycles to failure for the parts at major risk are presented in Figure 5. For this assessment the 40-lead side-brazed ceramic packages were found to be more likely to fail than the 132-pin Ceramic PGAs. The simulation prediction for the 40-lead side-brazed DIP was 4,270 cycles using the 10 °C to 67.5 °C simplified temperature range, 67.5 °C being the mid point between the average peak temperature 75 °C and the cruise temperature of 60 °C. Four years to failure was estimated if the assembly was subjected to three cycles per day or 5.8 years if the assembly was subjected to two cycles per day.

![Figure 5: Cycles to failure for selected electronic packages](image)

The first field failures were observed after 7 years of service becoming significant after 12 years. Root cause analysis showed the failures to be due to fatigue cracking of the through hole solder joint at the corners of the 40-lead side-brazed DIP. Figure 6 shows two photographs of a microsection of a typical failing joint. Figure 6.a shows the full PTH soldered joint with the side-brazed package, the lead clinched to ensure retention of the device during soldering and heat plate visible between the board and the device package. Figure 6.b is a higher magnification showing the solder cracking around the lead of the device.

![Figure 6: Microsection of failing joint](image)

5.3. Sensitivity to Temperature Range and Lead Configuration

To determine the sensitivity of the life prediction to details of the service profile, the assessment was repeated with temperature ranges of 10 °C to 60 °C, 10 °C to 67.5 °C and 10 °C to 75 °C, assuming 130 minutes dwell for each condition. Results of this assessment for the 40-lead side-brazed DIP packages are shown in Table 3. As presented in Table 3, the life of the CDIP dropped from ranging from...
6,160 to 3,090 cycles as the temperature range changed from 50 to 65 °C.

It should be noted that the 40-lead side-brazed DIP, as well as being the largest package, had side-brazed leads as opposed to a standard formed leads. The standard formed leads were found to provide a greater degree of compliance and packages with these leads exhibit longer service life. Simulations of a change in lead configuration from brazed to a standard formed lead indicated a 25 % longer life joint life. The results of this assessment are presented in Table 4.

Table 3: Cycles to failure for 40-lead side-brazed DIP for different temperature cycle ranges

<table>
<thead>
<tr>
<th>TEMPERATURE RANGE</th>
<th>10°C to 60°C</th>
<th>10°C to 67.5°C</th>
<th>10°C to 75°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycles To Failure 40-lead side-brazed DIP</td>
<td>6,160</td>
<td>4,270</td>
<td>3,090</td>
</tr>
</tbody>
</table>

Table 4: Dependence of cycles to failure on lead configuration

<table>
<thead>
<tr>
<th>LEAD CONFIGURATION</th>
<th>SIDE-BRAZED LEAD</th>
<th>REGULAR CERDIP STYLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycles To Failure 40-lead side-brazed DIP</td>
<td>4,270</td>
<td>5,780</td>
</tr>
<tr>
<td>Cycles To Failure 20 DIP</td>
<td>13,700</td>
<td>17,600</td>
</tr>
</tbody>
</table>

The reasonable agreement seen between the test and service results and the simulated values for cycles to failure gives confidence in the use of the models and potentially greater confidence in the factorial difference in cycles to failure between the different packages. Consequently an estimate of when the other packages may be expected to exhibit failures in service can be made with some confidence. In addition, the cycles to failure values obtained from the simulation can be used to determine acceleration factors (AF). The acceleration factors are obtained by dividing the predicted number of cycles to failure under service over the predicted number of cycles to failure under test conditions. AF in combination with test data is the best method for approximating field life.

For this study, the 40-lead side-brazed DIP has an AF of 3, which means that 7,000 cycles to failure under usage conditions can be accelerated to ~ 2,333 cycles during the test profile (or 16,230 to 5,410). The PGA132 has an AF of 3.7, which means that the 4,000 cycles to failure under testing conditions is equal to ~ 14,800 cycles during the usage profile or 7,800 cycles after the 40-lead side-brazed DIP fails. Calibrating the simulation results of the DIP28 (next component at risk of failure on the fielded computer card) under usage conditions with the ratio of the predicted values over the field failures gives an estimate of the number of cycles to failure close to 19,508 cycles or approximately 12,508 cycles (or 17 years for 2 cycles/day) remaining after the 40-lead side-brazed DIP fails which is well beyond the design life of the product.

The sensitivity to temperature range and the dependence on lead configuration also give significant guidance on how much margin should be allowed at the design stage and on future package style selection for this failure mode. Damage to the solder interconnects due to vibration, intermetallic growth, or exposure to corrosive environment was not considered. It should also be noted that the results of this assessment do not attempt to quantify the impact of the conformal coating or potting on the durability of the package to board interconnects. Nominal dimensions were used in this assessment and good manufacturing quality was assumed. Further, failure of the packaged devices and other failure mechanisms were not considered. The risk related to failure mechanisms other than interconnect durability on a well-designed board is expected to be relatively low. However, accelerated testing is strongly recommended to provide validation for the assumptions made in this evaluation and to assure that unexpected failure risks are not present.

7. ACKNOWLEDGEMENT

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REFERENCES


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