Project Title: Identifying Precursors to Failure for Insulated Gate Bipolar Transistors (IGBTs)

CALCE Team: Nishad Patil, Myra Torres and Dr. Diganta Das

Objectives: To identify precursors to failure for IGBTs using physics of failure methods and models.

Introduction:

The industry consensus is that the trend towards more electric aircraft will result in increased use of power semiconductor devices. Power semiconductor devices also find increased use in the automotive industry particularly in the hybrid and electric vehicles. In all these circumstances, power semiconductor failure or degradation can be costly. Failure of course, can result in complete loss of power and may even have safety consequences. Degradation of the devices can also result in reduced efficiency, thereby defeating the purpose of the power systems. The Insulated Gate Bipolar Transistor (IGBT) is a power transistor that combines fast switching speeds of the MOSFET with high current capability of bipolar transistors. IGBTs are replacing and supplementing power MOSFETs in sectors such as avionics, industrial, and automotive for power conversion and motor speed control. It is necessary to be able to predict when a maintenance action will be necessary during the operation of the power electronics modules which incorporate power semiconductor devices such as the Insulated Gate Bipolar Transistors (IGBT).

Approach:

The precursor monitoring approach to prognostics involves monitoring changes in parameters, which are then associated with a particular type of failure. The failure is predicted by correlating the change in the monitored parameters with the associated degradation in the device. The precursor monitoring approach is used for identifying the parameters to be monitored. Since there are different failure signatures for different failure mechanisms, a list of critical failure mechanisms and the associated electrical parameters (failure signatures) to be monitored are created through a failure mode, mechanisms, and effects analysis (FMMEA).

FMMEA is a methodology to identify potential failure mechanisms and models for all potential failures modes, and to prioritize failure mechanisms. The output of the FMMEA process is a list of critical failure mechanisms that help us identify the precursors to monitor and the relevant physics of failure models to use to predict remaining life of the component.

Critical transistor failure mechanisms include hot electrons, gate-oxide breakdown, and latch-up. Gate oxide breakdown is one of the major concerns in power transistors. Damage to the gate oxide can result in excessive leakage current, increased standby power, and a increase in response time. The damage to the oxide will eventually cause a power transistor to short-circuit. The damage results from thinning of the oxide and an increase in the effective electric field. Two types of gate oxide breakdown are possible: A catastrophic breakdown can occur as the result of electrical overstress. Time-dependent dielectric breakdown (TDDB), takes place during operation within the rated conditions of voltage, temperature, and power dissipation. Time dependent dielectric breakdown refers to the damage accumulated in the gate oxide region of a power transistor during use within its rated operating condition. The rated operating conditions include voltage, temperature, and the magnitude of the electric field between the drain and body.

The failure modes for the IGBT can be in the form of degradation of certain key electrical parameters. For a working device, the failure mode of interest is functionality. In the device level analysis that is being undertaken now, failure mode will be degradation of electrical parameters such as on-state resistance, threshold voltage and switching characteristics .

The aging of the gate oxide is accelerated by the high temperature gate bias (HTGB) test. This test stresses the oxide-silicon interface by the application of an electric field at high temperature. The device under test is biased between the gate and emitter with $V_{GE} = V_{Stress}$, with the collector-emitter short-circuited.

As the power transistors age, their performance degrades. The drop in performance could generate failures in the systems in which the transistors operate. In this study, critical failure mechanisms in IGBTs will be evaluated. The electrical parameters that change due to aging effects will be monitored. This data along with physics of failure models will be used to generate a hybrid fault propagation model that will then be used to estimate remaining life of the device.

Deliverables:

- Identification of critical failure mechanisms for IGBT
- Identification of precursors to failure for the failure mechanisms identified
- Data on the evolution and trends of possible electrical precursors with time under temperature and gate bias conditions

Project Status:

High temperature gate bias tests have been performed for 744 hours on International Rectifier (IRG4BC30KD) IGBTs to accelerate the time dependent dielectric breakdown of the gate oxide. Three parameters, the threshold voltage, the collector-emitter on voltage and the transconductance were measured at periodic intervals to trace their evolution with time. Electrical parameters are being measured over a range of temperatures for aged and new IGBT parts to track effect of temperature on electrical parameters of aged and new parts. It is expected that the difference in magnitude between the electrical parameters of new and aged parts increases with temperature. Switching characteristics of the IGBTs will be measured across a broad range of frequencies. It is expected that changes in switching characteristics will be significant at higher frequencies. Test circuits and boards will be designed and fabricated to monitor additional parameters such as switching characteristics. In-situ monitoring of the electrical parameters will be performed at a higher stress temperature of 150^oC and higher gate voltage. The maximum rated gate voltage of 20 volts will be applied to accelerate TDDB. We call this new test high stress HTGB. Analysis of the data will be carried out to correlate changes in electrical parameters to degradation predicted by physics of failure models.

Estimated Schedule:

Tasks	Dec 2007	Jan 2008	Feb 2008	Mar 2008	Apr 2008
Design of test circuits and boards					
Determine effects of temperature on device characteristics					
Determine effects of frequency on device switching charatceristics					
Perform accelerated aging tests and monitor selected parameters in-situ					
Data analysis					
Report and review					
					▲